WHAT IS CLAIMED IS

1. A semiconductor integrated circuit, comprising:

a plurality of layers provided on a semiconductor substrate;

wires provided in a first layer that is one of said plurality of layers; and

wire dummies provided in a second layer different from the first layer and having an arrangement that avoids areas overlapping positions of said wires.

2. The semiconductor integrated circuit as claimed in claim 1, wherein the first layer is a layer immediately above or immediately below the second layer.

3. The semiconductor integrated circuit as claimed in claim 1, wherein said wires are signal wires excluding power supply wires.

4. The semiconductor integrated circuit as claimed in claim 3, wherein said wire dummies are further provided in areas overlapping positions of

said power supply wires that are provided in the first layer.

5. The semiconductor integrated circuit as claimed in claim 4, wherein said signal wires have a width less than a predetermined wire width, and said power supply wires have a width greater than the predetermined wire width.

6. The semiconductor integrated circuit as claimed in claim 1, wherein said wire dummies have the arrangement that further avoids areas overlapping positions of polysilicon or diffusion layers.

7. A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

dummy patterns provided in said wire layer and having different sizes.

8. The semiconductor integrated circuit as claimed in claim 7, wherein said dummy patterns having different sizes are arranged at respective

different pattern intervals.

9. A semiconductor integrated circuit, comprising:

a wire layer;

wires provided in said wire layer; and

dummy patterns provided in said wire layer and having different shapes conforming to patterns of said wires.

10. A semiconductor integrated circuit, comprising:

a plurality of wire layers stacked one over another;

a plurality of wires including first wires and second wires and arranged in a first wire layer that is one of said wire layers, said plurality of wires being arranged at various intervals, a shortest of which is a predetermined interval, said first wires having wires on both sides thereof at a distance equal to said predetermined interval, and said second wires having no wires on both sides thereof at a distance equal to the predetermined interval; and

dummy patterns provided in a second wire layer immediately above or below the first wire layer, said dummy patterns being arranged in areas overlapping positions of said first wires and being absent in areas overlapping positions of said second wires.

11. The semiconductor integrated circuit as claimed in claim 10, wherein said plurality of wires includes third wires having a wire only on one side thereof at a distance equal to the predetermined interval, and said dummy patterns are arranged in the second layer in areas overlapping positions of said third wires.

12. The semiconductor integrated circuit as claimed in claim 10, wherein said plurality of wires includes third wires having a wire only on one side thereof at a distance equal to the predetermined interval, and said dummy patterns are absent in the second layer in areas overlapping positions of said third wires.

13. A semiconductor integrated circuit, comprising:

a plurality of wire layers stacked one over another;

a plurality of wires including first wires, second wires, and third wires, and arranged in a first wire layer that is one of said wire layers, said first wires being narrower than a predetermined width, said second wires being equal to or wider than the predetermined width and carrying a power supply potential, and said third wires being equal to or wider than the predetermined width and

carrying a clock signal; and

dummy patterns provided in a second wire layer immediately above or below the first wire layer, said dummy patterns being arranged in areas overlapping positions of said second wires and being absent in areas overlapping positions of said third wires.

14. A method of arranging dummy patterns, comprising the steps of:

providing sets of dummy patterns, each of said sets including patterns of a corresponding size arranged in rows and columns; and

arranging the sets of dummy patterns in a descending order of size on a wire layout.

15. A method of arranging dummy patterns, comprising the steps of:

providing dummy patterns arranged at varying intervals inclusive of first intervals and second intervals that are longer than the first intervals;

arranging the dummy patterns on a wire layout;

combining the dummy patterns spaced at the first intervals by expanding size of the dummy patterns; and

shrinking the size of the combined dummy patterns.

16. A method of arranging dummy patterns, comprising:

expanding width of first wire patterns arranged in a first wire layer at various intervals, a shortest of which is a predetermined interval, so as to combine the first wire patterns spaced at said predetermined interval;

shrinking width of the expanded wire patterns including the combined wire patterns;

generating second wire patterns by superimposing the shrunk wire patterns on the first wire patterns; and

arranging dummy patterns in a second layer immediately above or below the first layer while avoiding areas overlapping positions of the second wire patterns, except for positions of the shrunk wire patterns.